REMARKS

The present amendment is submitted in response to the Final Office Action mailed March 17, 2009. In view of the amendments above and the remarks to follow, reconsideration and allowance of this application are respectfully requested.

Status of Claims

Claims 1-16 are pending in the application. Claims 1-2, 6-8 and 14-16 are amended.

Drawing Objection

In the Office Action, the drawings were objected to because they are blurry and difficult to read. Applicants believe that the drawings were probably blurred during transmission and will retransmit the drawings in compliance with the Examiner's request.

Rejections under 35 U.S.C. §112

In the Office Action, Claims 1-16 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as his invention. Claims 1, 7, 8, 14, 15 and 16 have been amended in a manner which is believed to overcome the rejections.

Rejections under 35 U.S.C. §102(b)

In the Office Action, Claims 1-4, 6-8, 10, and 12-14 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,768,742 ("Godfrey"). Applicant respectfully traverses the rejection.

Claims 1-4 are allowable

The cited portions of Godfrey do not anticipate claim 1 because the cited portions of Godfrey do not teach every element of claim 1. For example, the cited portions of Godfrey do not disclose or suggest, "*wherein a message issued by a first module M comprises first information indicative of a location of one of said modules S being addressed within the network, and second information indicative of a particular location within the addressed module S, such as a memory, or a register address*", as recited in claim 1. Instead Godfrey teaches that two internetworked-chip module addresses (i.e., ICMAs), shown as examples of network addresses that can be selected to accomplish on-chip and off-chip data transfers, comprises a plurality of network identifier bits and a number of bits to enable the network to identify the specific module 30 when a data packet arrives at that network. In other words, Godfrey identifies the network and a module within the network. In contrast to Godfrey, the invention goes beyond the identification of a network and a module within the network, by further identifying a particular location within an addressed module, such as a memory or a register address (i.e., using second information). It is respectfully submitted that Godfrey does not teach or suggest the use of second information to identify a particular location within an addressed module, such as a memory or a register address, as recited in claim 1. As discussed at par. 12 of the Application, the second information may invoke a particular response of the addressed module. Accordingly, Godfrey does not teach *wherein a message issued by a first module M comprises first information indicative of a location of one of said modules S being addressed within the network, and second information indicative of a particular location within the addressed module S, such as a memory, or a register address*", as recited in claim 1.

Further, Godfrey does not disclose "at least one address translation means for receiving said message issued by said first module M comprising said first and second information and arranging the first and the second information as a single address", as recited in claim 1. Rather, Godfrey discloses that data blocks are converted into data

packets. Specifically, Godfrey discloses that a protocol analyzer unit 44 may convert a data block into a number of data packets, or a plurality of data blocks into a single data packet.... for sender as well as receiver modules. See Godfrey, Col. 8, lines 42-46. It is respectfully submitted that converting a **data** block into a number of **data** packets is different from arranging first and second information as a single address on two levels. First, converting a single large block into a number of smaller blocks is different from combining two addresses into a single address. They are inverse operations. Secondly, Godfrey is teaching the conversion of data and not addresses. Accordingly, Godfrey does not teach *wherein a message issued by a first module M comprises first information indicative of a location of one of said modules S being addressed within the network, and second information indicative of a particular location within the addressed module S, such as a memory, or a register address*", as recited in claim 1. Therefore, claim 1 is allowable.

Claims 2-4 depend from claim 1, and are therefore allowable at least by virtue of their dependence from allowable claim 1.

Further the dependent claims recite additional features are not disclosed or suggested by the cited portions of Godfrey. For example, the cited portions of Godfrey do not disclose an integrated circuit comprising: at least one interface means associated to one of the modules for managing communication between one of said associated modules and the network, wherein one of said address translation means is arranged in one of said interface means, as in claim 2. The Office Action asserts that col. 8, lines 39-49 and Fig. 5 discloses this feature. See Office Action, page 6. However, Godfrey does not disclose an integrated circuit comprising at least one interface means and an address translation means arranged in one of the interface means. Instead, Godfrey discloses a module 30, as shown in Fig. 5, where each module 30 preferably includes a bus interface logic (BIL) 42, a protocol analyzer and an I/O Buffer 44, and various logic/memory

elements 46 coupled to one another. As discussed above, the protocol analyzer is different from an address translation means. For this additional reason, claim 2 is allowable.

As a further example of a dependent claim that recites additional features not disclosed or suggested by the cited portions of Godfrey, it is respectfully submitted that the cited portions of Godfrey do not disclose an integrated circuit wherein said address translation means comprises an address mapping table configured to store relations between global and local memory mapping, as in claim 4. The Office Action asserts that col. 2, lines 16-18, col. 6, lines 60-67 and col. 8, lines 50-52 disclose this feature. See Office Action, pages 6-7. However, Godfrey does not disclose an integrated circuit wherein said address translation means comprises an address mapping table configured to store relations between global and local memory mapping. Instead, Godfrey discloses that one or modules may operate as a DNS server and have a built in ICMA dictionary for the modules on the chip (see col. 2), mapping of Internet addresses to physical host addresses (col. 6) and a module serving as a network interconnect when the module's routing table is assigned values for available routes (col. 8). However, Godfrey does not disclose that every address in a slave has a global address and a local address. The global address relates to address as seen from the processing on the master M and the local address relates to the address of the slave. The address range of the global address may be 0000-FFFF, while a range within a slave may be 000-FFF. As described at pars. 40-42 of the application, the global address may be formed in different ways. Firstly, it is constituted by a network address and a local address. The network address may be the port identifier of the receiving module, i.e. the port ID of the passive network interface ports PNIP. Such a scheme would be backward compatible. Secondly, the global address is constituted by a connection identifier (connection id) and a local address as minimum information or alternatively the connection identifier, the passive network interface ports PNIP and the local address. The provision of the passive network interface ports PNIP is

in some cases redundant but increases the safety of the scheme. In the case of a master, a connection id identifies several slaves, and there should be some means to select one of them. The network interface port NIP address or global address (from which a passive network interface port PNIP id is derived) are still needed. In both cases (i.e., network interface (NI) address and global address), checks as means for selection are possible, as only a subset of the network interface ports NIPs are mapped to the connection. Hence, address translation is performed based on a connection id + global address, i.e. on the passive network interface port PNIP id and the local address, possibly also with communication properties of the connection and check.

Claims 6-8, 10 and 12-14 are allowable

Independent Claim 6 recites similar subject matter as Independent Claim 1 and therefore contain the limitations of Claim 1. Hence, for at least the same reasons given for Claim 1, Claim 6 is believed to recite statutory subject matter under 35 USC 102(e).

Claims 7-8, 10 and 12-14 depend from claim 6, which Applicant has shown to be allowable. Hence, claims 7-8, 10 and 12-14 are therefore allowable at least by virtue of their dependence from allowable claim 6.

Claim 5 is allowable

In the Office Action, Claim 5 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Godfrey in view of U.S. Patent No. 6,381,638 ("Mahler"). Applicants respectfully traverse the rejection.

As explained above, the cited portions of Godfrey do not disclose or suggest each and every element of claim 1 from which claim 5 depends. The cited portions of Mahler do not disclose each of the elements of claim 1 that are not disclosed by Godfrey. For example, Mahler does not disclose or suggest "*wherein a message issued by a first*

module M comprises first information indicative of a location of one of said modules S being addressed within the network, and second information indicative of a particular location within the addressed module S, such as a memory, or a register address", as recited in claim 1. Instead, Mahler is cited by the Office for allegedly disclosing an address mapping table containing fields for every channel of a connection, for network interface ports of a connection and for local addresses in addressed modules. However, it is respectfully submitted that Mahler does not disclose an address mapping table containing fields for every channel of a connection, for network interface ports of a connection and for local addresses in addressed modules. Mahler, merely discloses a mapping table including columns for **an external network address**, a **TCP port** and an **OBAR ID.** Applicants respectfully submit that this is different from an address mapping table containing fields for **every channel of a connection**, for network interface ports of a connection and **for local addresses in addressed modules**, as recited in claim 5. Paragraph 38 of the application recites that the address mapping table AMT can be implemented on a static, programmable or dynamic basis and may contain fields for every channel of a connection, for the connection identifier, for network interface ports ANIP, PNIP of a connection, and/or for local addresses in addressed modules S.

Therefore, the cited portions of Godfrey and Mahler fail to disclose or suggest each and every element of claim 1, or of claim 5, by virtue of its dependence from claim 1. Hence, claim 5 is allowable.

Claim 15 is allowable

In the Office Action, Claim 15 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Godfrey in view of U.S. Patent No. 6,018,782 ("Hartmann"). Applicants respectfully traverse the rejection.

As explained above, the cited portions of Godfrey do not disclose or suggest each and every element of claim 6 from which claim 15 depends. The cited portions of Hartman do not disclose each of the elements of claim 6 that are not disclosed by Godfrey. For example, Hartmann does not disclose or suggest "*wherein a message issued by a first module M comprises first information indicative of a location of one of said modules S being addressed within the network, and second information indicative of a particular location within the addressed module S, such as a memory, or a register address*", as recited in claim 6. Instead, Hartmann is cited by the Office for allegedly disclosing that the at least one network interface comprises at least two network interface ports to allow a module associated with said at least one network interface to communicate with a router network or at least one other module from among said plurality of modules.

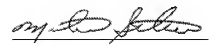
Therefore, the cited portions of Godfrey and Hartmann fail to disclose or suggest each and every element of claim 6, or of claim 15, by virtue of its dependence from claim 6. Hence, claim 15 is allowable.

Conclusion

In view of the foregoing amendments and remarks, it is respectfully submitted that all claims presently pending in the application, namely, Claims 1-16 are believed to be in condition for allowance and patentably distinguishable over the art of record.

If the Examiner should have any questions concerning this communication or feels that an interview would be helpful, the Examiner is requested to call Mike Belk, Esq., Intellectual Property Counsel, Philips Electronics North America, at 914-945-6000.

Respectfully submitted,



Michael A. Scaturro
Reg. No. 51,356
Attorney for Applicant

Mailing Address:
Intellectual Property Counsel
Philips Electronics North America Corp.
P.O. Box 3001
345 Scarborough Road
Briarcliff Manor, New York 10510-8001